IN THE CLAIMS

**Please amend the claims as follows:**

1. (Currently Amended) In a computer-aided design and verification system, a method for facilitating signal override in a simulation model of a digital circuit design that includes one or more design entities described utilizing a hardware description language (HDL), said method comprising:

instantiating an instrumentation entity within at least one of said one or more design entities using port mapping fields designated by a non-conventional HDL comment syntax, said non-conventional HDL comment syntax processed by a post-compiler instrumentation load tool to instantiate said instrumentation entity during a post-compile model build process, wherein said non-conventional HDL comment syntax is recognized by an HDL compiler such that the HDL compiler does not instantiate said instrumentation entity into the digital circuit design, said port mapping fields further including:

an input port mapping field containing data representing an input port at which said instrumentation entity receives a designated signal to be overridden; and

an output port mapping field comprising an override signal field specifying the name of said override signal, a port name field specifying the name of the port from which said override signal is output from said instrumentation entity, and a target signal field specifying the name of said designated signal to be overridden;

generating signal selection means within said simulation model for selectively overriding said designated signal with said override signal responsive to said post-compiler instrumentation load tool processing said port mapping fields; and

wherein said output port mapping field further comprises a control port field specifying an output port for delivering an override enable signal to said signal selection means.

2. (Canceled)

3. (Canceled)

4. (Currently Amended) The method of claim [[2]] 1, further comprising:



PAGE 3/7 * RCVD AT 3/1/2006 5:44:33 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-3/5 * DNIS:2738300 * CSID:5123436446 * DURATION (mm-ss):02-42

instantiating a latch within said simulation model, wherein said latch stores an override disable bit; and

combining said override disable bit with said override enable signal within a logic gate to produce a combined selection signal that determines whether or not said signal selection means overrides said designated signal with said override signal.

5. (Currently Amended) In a computer-aided design and verification system, a system for facilitating signal override in a simulation model of a digital circuit design that includes one or more design entities described utilizing a hardware description language (HDL), said system comprising:

processing means for instantiating an instrumentation entity within at least one of said one or more design entities using port mapping fields designated by a non-conventional HDL comment syntax, said non-conventional HDL comment syntax processed by a post-compiler instrumentation load tool to instantiate said instrumentation entity during a post-compile model build process, wherein said non-conventional HDL comment syntax is recognized by an HDL compiler such that the HDL compiler does not instantiate said instrumentation entity into the digital circuit design, said port mapping fields further including:

an input port mapping field containing data representing an input port at which said instrumentation entity receives a designated signal to be overridden; and

an output port mapping field comprising an override signal field specifying the name of said override signal, a port name field specifying the name of the port from which said override signal is output from said instrumentation entity, and a target signal field specifying the name of said designated signal to be overridden;

processing means for generating signal selection means within said simulation model for selectively overriding said designated signal with said override signal responsive to said post-compiler instrumentation load tool processing said port mapping fields; and

wherein said output port mapping field further comprises a control port specifying an output port for delivering an override enable signal to said signal selection means.

6. (Canceled)



PAGE 4/7 * RCVD AT 3/1/2006 5:44:33 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-3/5 * DNIS:2738300 * CSID:5123436446 * DURATION (mm-ss):02-42

7. (Canceled)

8. (Currently Amended) The system of claim [[6]] 5, further comprising:

processing means for instantiating a latch within said simulation model, wherein said latch stores an override disable bit; and

processing means for combining said override disable bit with said override enable signal within a logic gate to produce a combined selection signal that determines whether or not said signal selection means overrides said designated signal with said override signal.

9. (Currently Amended) In a computer-aided design and verification system, a computer program product for facilitating signal override in a simulation model of a digital circuit design that includes one or more design entities described utilizing a hardware description language (HDL), said computer program product including computer-executable instructions for performing a method comprising:

instantiating an instrumentation entity within at least one of said one or more design entities using port mapping fields designated by a non-conventional HDL comment syntax, said non-conventional HDL comment syntax processed by a post-compiler instrumentation load tool to instantiate said instrumentation entity during a post-compile model build process, wherein said non-conventional HDL comment syntax is recognized by an HDL compiler such that the HDL compiler does not instantiate said instrumentation entity into the digital circuit design, said port mapping fields further including:

an input port mapping field containing data representing an input port at which said instrumentation entity receives a designated signal to be overridden; and

an output port mapping field comprising an override signal field specifying the name of said override signal, a port name field specifying the name of the port from which said override signal is output from said instrumentation entity, and a target signal field specifying the name of said designated signal to be overridden;

generating signal selection means within said simulation model for selectively overriding said designated signal with said override signal responsive to said post-compiler instrumentation load tool processing said port mapping fields; and

wherein said output port mapping field further comprises a control port field specifying



PAGE 5/7 * RCVD AT 3/1/2006 5:44:33 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-3/5 * DNIS:2738300 * CSID:5123436446 * DURATION (mm-ss):02-42

an output port for delivering an override enable signal to said signal selection means.

10. (Canceled)

11. (Canceled)

12. (Currently Amended) The computer program product of claim [[10]] 9, wherein said method further comprises:

instantiating a latch within said simulation model, wherein said latch stores an override disable bit; and

combining said override disable bit with said override enable signal within a logic gate to produce a combined selection signal that determines whether or not said signal selection means overrides said designated signal with said override signal.

13. (Canceled)

14. (Canceled)

15. (Canceled)



PAGE 6/7 * RCVD AT 3/1/2006 5:44:33 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-3/5 * DNIS:2738300 * CSID:5123436446 * DURATION (mm-ss):02-42